REMARKS

Favorable reconsideration of this application in view of the following remarks is respectfully requested.

Claims 1-13 are pending in this application. Claims 1-13 have been amended to better characterize the present invention without the introduction of any new matter.

The outstanding Office Action includes an objection to Claim 11, a rejection to Claims 1-3, 5-10, 12, and 13 as being anticipated under 35 U.S.C. § 102(b) by Takashi (JP 1267617), a rejection of Claim 11 under 35 U.S.C. § 102(e) as being anticipated by Kim et al (U.S. Patent No. 6,191,831, Kim), and a rejection of Claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Takashi.

Turning first to the objection to Claim 11, it is noted that the insulating film has now been provided proper antecedent basis by the present amendment. Accordingly, it is believed that this objection should be withdrawn.

Before turning to the outstanding prior art rejections, it is believed that a brief review of the present invention would be helpful. In this regard, a first aspect of the present invention is concerned with a liquid crystal display having a gate electrode line that is formed on an insulating substrate with a source electrode line that includes a source electrode portion that intersects with the gate electrode line over an insulating film. A thin film transistor is located in the vicinity of a portion in which the gate electrode line is intersected by the source electrode line and there are two drain electrode lines that include drain electrode portions of the thin film transistor. The drain electrode lines are connected with a pixel electrode while the portions of the drain electrode lines forming the two drain electrodes have a near side that is facing a source electrode overlapping the gate electrode line while a far side opposed to the

near side does not overlap the gate electrode line. The arrangement reduces the capacitance between the drain electrodes and the gate electrode line.

Another aspect of the invention relates to the method of making the display.

Turning to the rejection of Claims 1-3, 5-10, 12, and 13 based upon anticipation by Takashi, it is noted that this references does not have the claimed drain electrodes having the near sides thereof facing a source electrode superimposed over a gate electrode with the far sides of each drain electrode opposed to the near side not being superimposed over the gate electrode. Clearly, both the near sides and far sides of the Takeshi drain electrodes overlap the gate electrode line as shown in relied upon Figure 1(a). This is purposely done by Takashi to provide for wide variance in the positioning the gate electrodes as illustrated in Figures 5(a)-(e).

Turning to the rejection of Claim 11 as being anticipated by Kim, it is clear that this patent fails to disclose the drain electrodes having a near side that is superposed with the gate electrode and that faces the source electrode and a far side opposed to the near side that is not so superposed. In this regard, the common electrode for the drain between the two gates overlaps both gates. Thus, there is no anticipation.

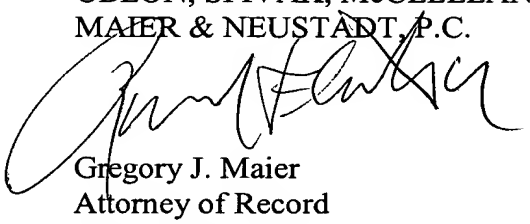
Finally, as to the obviousness rejection applied to Claim 4, the rejection offers an unsupported conclusion as to what is conventional in film transistor manufacture where such conclusions unsupported by evidence are clearly improper in light of recent court decisions such as In re Lee, 61 USPQ2d (Fed. Cir. 2002). Thus, as the required evidence to support the improper assertions of knowledge in the art is lacking, the improper rejection should be withdrawn.

Accordingly, as none of the applied prior art rejections establish a *prima facie* case relative to the presently amended claims, withdrawal of these rejections is believed to be in order.

As no further issues are believed to remain outstanding in the present application, it is believed that this application is clearly in condition for formal allowance. Consequently, an early and favorable action to this effect is earnestly and respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Attorney of Record
Registration No. 25,599
Raymond F. Cardillo, Jr.
Registration No. 40,440

22850

(703) 413-3000
Fax No.: (703) 413-2220
GJM/RFC/cja

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Marked-Up Copy
Serial No: 09/832,892
Amendment Filed:
12-31-02

IN THE CLAIMS

--1. (Amended) A liquid crystal display comprising:

a gate electrode line including a gate electrode formed on an insulating substrate;

a source electrode line including a source electrode intersected with said gate electrode line via an insulating film;

a thin film transistor including said gate electrode, said source electrode, and two drain electrodes located in a vicinity of a portion in which said gate electrode line is intersected with said source electrode line;

two drain electrode lines, each including a portion acting as one of the two drain electrodes [in said thin film transistor], said two drain electrode [line] lines each being connected with a pixel electrode;

wherein [said thin film transistor includes] said two drain [electrode lines] electrodes are located on [both] opposite sides of said source electrode[;] with each of said two drain electrodes [are formed at a place where each end portion of said two drain electrode lines] having a near side opposed to said source electrode that is superposed with said gate electrode [line] and a far side opposed to the near side that is not superposed with said gate electrode.

2. (Amended) The liquid crystal display of Claim 1, wherein an area of a region where said gate electrode [line] is superposed with the near side of one of said two drain

[electrode lines] electrodes is substantially identical to an area of a region where said gate [line] electrode is superposed with the near side of the other one of said two drain [electrode lines] electrodes.

3. (Amended) The liquid crystal display of Claim 2, wherein a length of a region in a channel lengthwise direction of said thin film transistor where said gate electrode [line] is superposed with the near side of one of said two drain electrodes is substantially identical to a length of a region in a channel lengthwise direction of said thin film transistor where said gate electrode [line] is superposed with the near side of the other one of said two drain [electrode lines] electrodes.

4. (Amended) The liquid crystal display of claim 3, wherein said length of said [area] region in the channel lengthwise direction is such a length as to prevent [a] current characteristics from degradation in said thin to film transistor.

5. (Amended) The liquid crystal display of any one of claims 1, 2, 3 and 4, wherein said two drain [electrode is] electrodes are formed in whole part of one end of [said] each drain electrode line in a channel widthwise direction where said near side of each drain electrode [line] is superposed with said gate electrode line.

6. (Amended) The liquid crystal display of any one of claims 1, 2, 3 and 4, wherein said two drain [electrode is] electrodes are formed at a portion where a part of one end of [said] each drain electrode line in the channel widthwise direction forms each near side opposed to said source electrode that is superposed with said gate electrode [line] on both sides of said source electrode.

7. (Amended) The liquid crystal display of any one of Claims 1, 2, 3, and 4[, 5 and 6,] wherein a lead portion of said source electrode line extended to said source electrode from

said source electrode line is provided with a semiconductor film situated above or below said gate electrode line via an insulating film in reference to the insulating substrate.

8. (Amended) The liquid crystal display of any one of Claims 1, 2, 3, and 4[, 5, and 7,] wherein a lead portion of said source electrode line extended to said source electrode from said source electrode line is provided with a semiconductor film, said semiconductor film being situated above said lead portion of said source electrode line or below the same in reference to the insulating substrate.

9. (Amended) The liquid crystal display of any one of Claims 1, 2, 3, and 4[, 5, 6, 7 or 8,] wherein said two drain [electrodes opposed to said source electrode to on both sides of said source] electrode lines are connected with each other [in the] to form a single drain electrode line region [between said two drain electrode lines and said pixel electrode, said drain electrodes being] connected [with] to said pixel electrode [by a single part of said drain electrodes].

10. (Amended) The liquid crystal display of any one of Claims 1, 2, 3, and 4[, 5, 6, 7, 8 or 9,] wherein said drain electrode [line is] lines are formed of a same film as that of said pixel electrode.

11. (Amended) A method for manufacturing a liquid crystal display comprising steps of:

forming a gate electrode line pattern on an insulating substrate;

forming an insulating film covering said gate electrode line pattern;

forming a semiconductor film covering said gate electrode line pattern;

depositing a conductive film serving as source/drain electrodes on said insulating film; and

subjecting said deposited conductive film to patterning in such a manner that two drain [electrodes] electrode portions are formed [in a portion where each end of two drain electrodes] with a near side opposed to said source electrode that is superposed in a channel lengthwise direction with said gate electrode line [on both sides of said source electrode] and with a far side opposite to the near side in the channel lengthwise direction that is not superposed with said gate electrode line.

12. (Amended) A method for manufacturing a liquid crystal display comprising steps of:

depositing a conductive film on an insulating substrate serving as source/drain electrodes;

subjecting said deposited conductive film to patterning in such a manner that two drain electrodes are formed [in a portion where each part of the two drain electrode lines] extending in a channel lengthwise direction with near sides and opposite facing far sides, with only the near sides being [is] superposed with a gate electrode [line], said drain electrode lines being opposed to said source electrode [on] at both [side surfaces] near sides;

forming a semiconductor film on said source/drain electrodes;

forming an insulating film in such a manner as to cover said semiconductor film; and

forming a gate electrode pattern on said insulating film.

13. (Amended) The method of Claim 11 or 12, further comprising a step of forming a pixel electrode pattern connected with each [said] drain electrode, wherein [said] each drain electrode is formed in said step of forming said pixel electrode pattern.--

Docket No. 205975US-2

IN RE APPLICATION OF: TAKEHISA YAMAGUCHI, ET AL.

SERIAL NO: 09/832,892

FILED: APRIL 12, 2001

FOR: LIQUID CRYSTAL DISPLAY AND MANUFACTURING METHOD THEREFOR

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ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Transmitted herewith is an amendment in the above-identified application.

- ☐ No additional fee is required
- ☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.
- ■ Additional documents filed herewith: MARKED-UP COPY

The Fee has been calculated as shown below:

CLAIMS	CLAIMS REMAINING		HIGHEST NUMBER PREVIOUSLY PAID	NO. EXTRA CLAIMS	RATE	CALCULATIONS
TOTAL	32	MINUS	20	12	× $18 =	$216.00
INDEPENDENT	3	MINUS	3	0	× $84 =	$0.00
		☐ MULTIPLE DEPENDENT CLAIMS			+ $280 =	$0.00
		TOTAL OF ABOVE CALCULATIONS				$216.00
		☐ Reduction by 50% for filing by Small Entity				$0.00
		☐ Recordation of Assignment			+ $40 =	$0.00
					TOTAL	$216.00

- ■ A check in the amount of **$216.00** is attached.
- ■ Please charge any additional Fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.
- ■ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Registration No. 25,599
Attorney of Record
Raymond F. Cardillo, Jr.
Registration No. 40,440

22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 10/00)